REMARKS

This is a full and timely response to the non-final Office Action of June 23, 2005. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this Amendment, claims 1, 2, 7, 8, 10, and 23-37 are pending in this application. Claim 37 is newly added, and it is believed that this amendment adds no new matter to the present application.

Response to §103 Rejections

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, *e.g.*, *In Re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §102 as allegedly being obvious over *Knowles* (U.S. Patent No. 6,446,107) in view of *Taewhan* ("Arithmetic Optimization using Carry-Save-Adders"). Claim 1 presently reads as follows:

> 1. An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:
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> circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;
>
> a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if at a particular binary value, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the respective coded logical value is set***, and wherein the generate bit, if at the particular binary value, indicates that two of the bits of the respective coded logical value are set. (Emphasis added).

Applicant respectfully asserts that the combination of *Knowles* and *Taewhan* fails to suggest at least the features of claim 1 highlighted hereinabove. Therefore, the 35 U.S.C. §103 rejection of claim 1 is improper and should be withdrawn.

In rejecting claim 1, it is asserted in the Office Action that *Knowles* discloses:

"an apparatus (e.g. abstract and col. 9 line 59 – col. 10 line 10) for performing addition of propagate, kill, and generate recoded numbers... wherein the kill bit, if at a particular binary value (e.g. k = a+b in line 66 col. 9 wherein the kill goes ***low or 0*** only if a and b (are) zero), indicative that each of the bits of the respective coded logical value is not (set) wherein the propagate bit, if at the particular binary value (e.g. p = a exor b in line 65 col. 9 wherein the propagate bill goes ***high or 1*** only if either a or b is high), indicates that only one of the bits of the respective coded logical value is (set)..." (Emphasis added).

However, Applicant observes that the foregoing Office Action assertions establish conditions that cause the alleged "kill bit" and the alleged "propagate bit" to be at ***different*** binary values. In particular, the condition described for the alleged "kill bit" places the "kill bit" at a "low or 0," whereas the condition described for the alleged "propagate bit" places the "propagate bit" at a "high or 1." There is nothing in the cited art to suggest that the described conditions should place the alleged "propagate bit" and the alleged "kill bit" at the ***same binary value***. Thus, the

cited art fails to suggest at least "wherein the kill bit, if at ***a particular binary value***, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at ***the particular binary value***, indicates that only one of the bits of the respective coded logical value is set," as described by claim 1. (Emphasis added).

For at least the above reasons, Applicant respectfully asserts that the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 1. Therefore, the 35 U.S.C. §103 rejection of claim 1 should be withdrawn.

Claims 2, 23-25, 27-29, and 33

Claim 2 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view *Taewhan* and in view of *Miller* (U.S. Patent No. 5,706,323). Further, claims 23-25, 27-29 and 33 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Knowles* in view of *Taewhan*. Applicant submits that the pending dependent claims 2, 23-25, 27-29, and 33 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2, 23-25, 27-29, and 33 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 1.

For example, claim 33 recites "wherein only one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can simultaneously be at the particular binary value." Applicant respectfully asserts that such features are not suggested by the cited art. Accordingly, the 35 U.S.C. §103 rejection of claim 33 is improper and should be withdrawn, notwithstanding the allowability of independent claim 1.

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan*. Claim 7 presently reads as follows:

> 7. A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:
> receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;
> generating a third propagate, kill, and generate representation and a carry-out value responsive to the first and second propagate, kill, and generate representations;
> logically combining the third propagate, kill, and generate representation with the carry-in value to generate a sum value and a carry value; and
> providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations,
> wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if at a particular binary value, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the respective coded logical value is set***, and wherein the generate bit, if at the particular binary value, indicates that two of the bits of the respective coded logical value are set. (Emphasis added).

For at least reasons similar to those set forth hereinabove in the arguments for allowance of claim 1, Applicant respectfully asserts that the cited art fails to suggest at least the features of claim 7 highlighted above. Accordingly, the 35 U.S.C. §103 rejection of claim 7 is improper and should be withdrawn.

Claims 8, 10, 30, 32, and 37

Claims 8, 30, and 32 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view of *Taewhan*. Further, claim 10 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan* and in view of *Miller*. In addition, claim 37 has been newly added via the

amendments set forth herein. Applicant submits that the pending dependent claims 8, 10, 30, 32, and 37 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8, 10, 30, 32, and 37 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 1.

For example, similar to allowable claims 34 and 36, claim 37 recites "wherein each set bit of the logical value has a binary value of one." For at least the reasons that claims 34 and 36 are allowable, Applicant respectfully asserts that claim 37 is allowable.

Claim 35

Claim 35 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan*. Claim 35 presently reads as follows:

> 35. An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:
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> circuitry configured to receive an operand defining a logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit, wherein the logical value, when decoded into a non-PKG form, has a plurality of bits, ***wherein the kill bit, if at a particular binary value, indicates that none of the bits of the logical value are set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the logical value is set***, and wherein the generate bit, if at the particular binary value, indicates that two bits of the logical value are set; and
>
> a carry save adder configured to add the operand in PKG form to a carry bit without decoding the operand from PKG form. (Emphasis added).

For at least reasons similar to those set forth hereinabove in the arguments for allowance of claim 1, Applicant respectfully asserts that the cited art fails to suggest at least the features of

claim 35 highlighted above. Accordingly, the 35 U.S.C. §103 rejection of claim 35 is improper and should be withdrawn.

Allowable Subject Matter

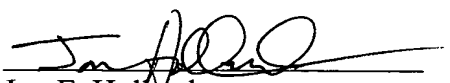
Claims 26, 31, 34, and 36 have been indicated as allowable by the outstanding Office Action if such claims are rewritten to include the limitations of their respective base claims. For at least the reasons set forth hereinabove, Applicant submits that the respective base claims 1, 7, and 35 are allowable and claims 26, 31, 34, and 36 are, therefore, allowable as a matter of law. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Accordingly, Applicant respectfully submits that claims 26, 31, 34, and 36 are allowable in their present form.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: 

Jon E. Holland
Reg. No. 41,077
(256) 704-3900 Ext. 103

Hewlett-Packard Development Company, L.P.
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400